REMARKS

This amendment is being filed along with a Request for Continued Examination (RCE) application in response to the final Office Action having a mailing date of April 17, 2006. Claims 1-3, 5, 10, 12-13, and 16 are amended as shown. New claims 17-23 are added. No new matter has been added. With this amendment, claims 1-23 are pending in the application.

The applicants thank the Examiner for double checking the application file to confirm that the certified copy of the priority document is missing. Therefore, a replacement copy of the certified copy has been or will be ordered, and will be filed in due course during the pendency of the present application.

I. Discussion of the Cited Reference

The final Office Action rejected claims 1-16 as being anticipated under 35 U.S.C. §102(e) by Allen (U.S. Patent No. 6,151,568). Furthermore, pages 3-5 of the final Office Action addressed the applicants' previous arguments. It is respectfully submitted that the claims are allowable given the amendments above and the remarks below.

To later assist in recognizing the differences between the claimed subject matter and the cited reference, a general discussion of Allen and the present applicants' disclosed embodiments are provided hereinafter.

Allen discloses a method for power estimation based on activity data, which results from simulation or activity estimation. According to column 2, lines 34-61, Allen disclose a tool that includes power modules, an analysis module, and a display device. The analysis module associates RTL elements in an electrical design with power modules. Additionally, the analysis module creates an interconnected set of components representative of the RTL elements and the connections between them. This interconnected set represents the power characteristics of the RTL elements.

Specifically and for example, as one can from Figure 3, Allen synthesizes the HDL description of a circuit to a lower abstraction level. It is noted that Allen creates an abstract syntax tree in which he searches for nodes, which are present in a technology library. This

technology library contains standard functional RTL blocks such as adders and memories in the case of RTL elements (*see, e.g.*, column 5, lines 40-61 of Allen).

After the association of a RTL block in the technology library to each node, Allen flattens the database and creates a so-called "scenario file," which describes the circuit. *See, e.g.*, column 7, lines 22-40 of Allen.

The blocks of the technology library are then associated (*see, e.g.*, column 6, lines 11-18 of Allen) to so-called "power modules" that contain the characteristic descriptions of the power consumption of that block (*see, e.g.*, column 7, line 59 to column 8, line 15 of Allen). Obviously therefore, these power modules are required in Allen to estimate the power consumption related to switching activity, pin capacitance, etc. It is clear that these power modules in Allen are in no way present in the actual circuit design and are only used to model the blocks found in his syntax tree.

In fact, Allen estimates the power consumption of a block from its "activity" data and from the description of the associated power module. *See, e.g.*, column 8, lines 52-60 of Allen.

Allen discloses some of his techniques to gather this "activity" data. One method according to Allen is to use simulation data, which might come from simulator module 74 in the analysis module 66 (*see, e.g.*, column 10, lines 25-30 of Allen) or from a GUI 68 (*see, e.g.*, column 11, lines 5-10 of Allen). Based on these simulation results, the activity data of a certain block can be estimated. Allen discusses some types of "activity" data in column 8, lines 31-59.

In the absence of simulation, Allen provides a method to estimate the activity data of a certain block from the interconnection of blocks and input activity. In detail, this method is disclosed in column 11, lines 17-67 of Allen.

In short, Allen discloses a method for estimating power consumption of blocks based on power consumption models of those blocks and activity data. These power consumption models are described by so-called "power modules." The power modules do not form part of the circuit itself, but rather are modeled based on a generated set of interconnections that represents power characteristics of RTL elements.

II. Discussion of the Applicants' Disclosed Embodiment(s)

A disclosed embodiment will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiment, and the discussion of the differences between the disclosed embodiment and subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences are intended to merely help the Examiner appreciate important claim distinctions discussed thereafter.

The present applicants have disclosed one or more embodiments in which activity data is obtained directly from a real circuit implementation. This means that the embodiment(s) use real circuit activity data, and not simulated or estimated ones as in Allen. In no way does Allen disclose, teach, or suggest the gathering of activity data directly from a real circuit implementation. As explained above, Allen gathers his activity data based on power consumption models.

To provide capability to obtain activity data in real circuits, the present applicants' embodiments include additional modules B, which might be for example coupled to the output pins of a functional block G. In this way, the modules B are able to gather the number of transitions performed by the associated functional block G. To read the data from those modules B, hardware emulators may be used to read the content of certain memory addresses.

The modules B of an embodiment perform an emulation of the digital circuit described by the functional block G. A real circuit implementation on which emulation is performed (*e.g.*, the present applicants' embodiments) differs from a layout abstraction layer on which simulation is performed (*e.g.*, Allen). Allen is completely silent as to an emulator coupled to the digital circuit at the hardware level of the digital circuit to gather activity information of the digital circuit.

Moreover and as explained above, Allen uses the abstraction level in order to generate an interconnected set of components, representative of the RTL elements and the connections between them. The interconnected set of components represent power characteristics of the RTL elements, and the components are associated with Allen's power modules. *See, e.g.*, column 2, lines 40-54 of Allen. Since the interconnected set of Allen is

generated from RTL elements, the interconnected set is inherently at a different level than the RTL elements and/or the actual digital circuit.

Page 4, paragraph 2b of the final Office Action has interpreted the power modules of Allen as being the same as the present applicants' additional element B. However, these power modules of Allen are models (in the software), which describe the power consumption of a certain block. In fact, in column 8, lines 36-60, Allen illustrates a power module that describes the power consumption characteristics of a memory. For example, he speaks of a list, which describes the transitions and the energy consumption of each transition.

In contrast, the present applicants' embodiment(s) uses the additional element B that is directly inserted in the hardware level of the digital circuit. Additionally, the additional element B (which may take the form of an adder or counter or other suitable hardware level element) performs not a descriptive function (such as the power module of Allen), but rather gathers the number of transitions of the digital circuit during operation of the digital circuit. In short, Allen in no way discloses, teaches, or suggests the use of activity data being gathered from real hardware activity in real time, using an additional element that has been coupled to the digital circuit at the hardware level of the digital circuit.

Moreover, the additional elements B are inserted directly in the hardware level of the digital circuit to modify and form a part of the digital circuit, without modification of the original functionality of the digital circuit. *See, e.g.*, page 3, lines 10-14; page 6, lines 21-24; page 8, lines 15-17; and elsewhere in the present application.

III. Discussion of the Claims

The various claims are amended as shown above to more precisely recite at least some of the distinctions discussed above. The claims will be discussed in turn below.

Independent claim 1 is amended to recite, *inter alia*, "emulating, at said hardware level, the digital circuit using additional elements associated to and coupled to said functional element at said hardware level." Allen does not disclose, teach, or suggest these features. For example and as explained above, the final Office Action has interpreted the "power module" of Allen as the claimed "additional elements."

However and as explained above, the power module of Allen does not emulate his digital circuit at the hardware level of his digital circuit. Rather, his power modules are used to model the blocks in his syntax tree. More specifically, his power modules are associated with a set of interconnects that represent power characteristics of RTL elements. His power modules are therefore implemented in software that simulates at a different level of abstraction (*e.g.*, at the level of the generated set of interconnects) than the hardware level of his original digital circuit. As such, Allen does not meet the limitations of claim 1 that recite "emulating, at said hardware level, the digital circuit ..." Therefore, claim 1 is allowable over Allen.

Also as explained above, Allen associates his power modules to the interconnected set of components. Therefore, his power modules are not "coupled to said functional element at said hardware level" as recited in claim 1. That is, claim 1 states that the digital circuit is described "at the hardware level" using the functional element and that the additional elements are coupled to the functional element at that same said "hardware level." These limitations cannot be met by Allen. His digital circuit is at some hardware level; his set of interconnections are at some other (different) hardware level, since the set of interconnects has been generated from the RTL elements; and his power modules are associated with the set of interconnects, which are at a different level than his original digital circuit. Therefore, claim 1 is further allowable over Allen.

Claim 1 further recites "said additional elements being able to detect, during emulation of the digital circuit, at least one signal indicative of a behavior, and hence of power consumption ...," and further recites (as amended) "acquiring a value of said at least one signal during the emulation of the digital circuit." Allen does not disclose, teach, or suggest detection and acquiring during emulation of his digital circuit as recited in claim 1. Allen detects the number of transitions based on simulation results (*i.e.*, the activity data explained above). Allen states on column 11, lines 11-12 that the "power estimations are performed when activity data is acquired from simulation for every node ..." (emphasis ours). Thus, Allen can only obtain his activity data after completion of the simulation and not during simulation. Also, Allen's technique does not even involve detection during actual circuit operation, since he is performing a simulation. Accordingly, claim 1 is yet further allowable over Allen.

The various dependent claims that depend upon claim 1 also contain distinctive recitations. For example, claim 3 recites that the additional elements are able to obtain a count, a fraction of time, and the value during emulation of the digital circuit.

New dependent claim 17 recites "modifying said digital circuit at said hardware level by adding at least one of said additional elements to said functional element to allow said added additional element to form part of said digital circuit at said hardware level, without modification of an original functionality of said digital circuit." None of these features are disclosed, taught, or suggested by Allen. His power modules are simply associated to a model that is based on a generated set of interconnects, and are in no way modifying and forming part of his digital circuit, without modification of an original functionality of his digital circuit. Accordingly, claim 17 is allowable.

New dependent claim 18 recites "detecting, during operation of said digital circuit, said number of transitions." It is true that Allen detects a number of transitions. However, such transitions are performed by a simulation model and not by his digital circuit, and this number is based on simulation results that are obtained after performing the simulations. Instead, claim 18 recites detecting this number during the operation of the digital circuit. Therefore, claim 18 is allowable.

New dependent claim 19 recites "acquiring said value in real time." Support for this recitation can be found, for instance, on page 5, lines 5-8 of the present application. Allen cannot meet the limitations of claim 19, since he obtains his data after simulation is completed, and therefore is inherently not "real time." Claim 19 is thus allowable.

Independent claims 10 and 13 have been amended in a manner generally consistent with the amendments to independent claim 1. Thus, claims 10 and 13 are allowable.

New dependent claims 20-23 have been added. These dependent claims recite subject matter generally consistent with the recitations in dependent claims 17-18, and are allowable.

The various claims are further amended as shown above to make their language consistent with the amended independent claims and/or to otherwise place such claims in better form. The appropriate fee to cover payment of the new claims is included herewith.

IV. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the applicants' attorney Dennis M. de Guzman has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact Mr. de Guzman at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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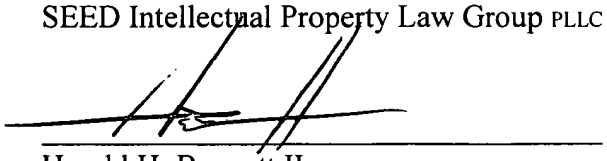

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